

# **Evaluating Support for OpenMP Offload Features**

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### Abstract

OpenMP has evolved to meet the rapid development hardware platforms including heterogenous programming. DOE applications tend to push the bleeding edge of features ratified in the OpenMP specification and tend to expose the rough edges of the features' implementations. The software harness on DOE supercomputers (e.g. Titan and Summit) include Cray, Clang, Flang, XL and GCC compilers which claim partial support for the latest features in OpenMP 4.0+. This work focuses on evaluating such support across compiler implementations, focusing on OpenMP 4.5 target offload directives. Our preliminary evaluation consist of a tests suite, as well as performance comparison.

Our tests not only evaluate the OpenMP implementations but also expose ambiguities in the OpenMP 4.5 specification. We see this as a synergistic effort to help identify and correct features that are required by DOE applications and prevent deployment delays later on.

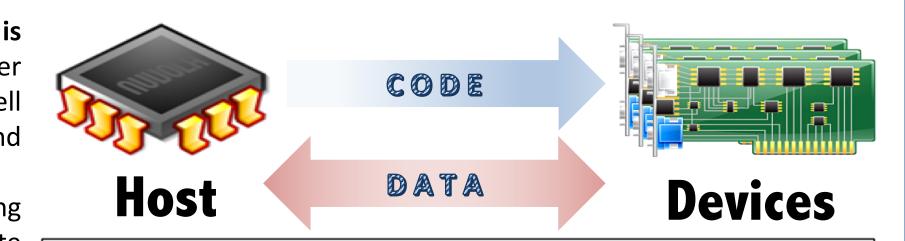
**OpenMP** abstract machine for offloading features is **host centric:** Offloading directives hint the compiler to create device executable regions of code, as well as code and data movement between host and device.

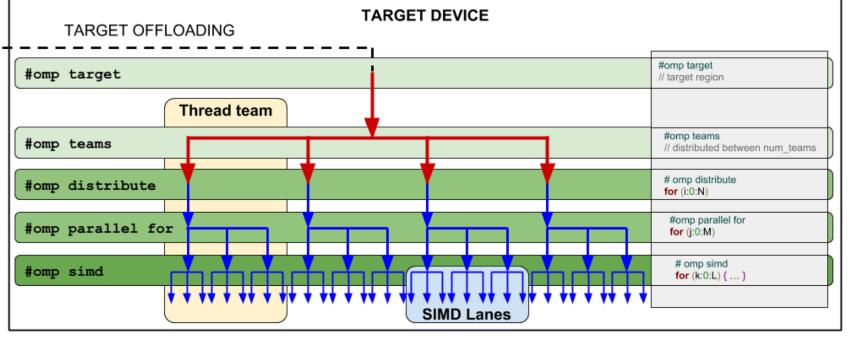
OpenMP frees the programmer from bookkeeping data allocation and movement, as well as separate compilation of code for host and device.

OpenMP 4.5 in particular provides more control to the programmer to handle data movement between host and device.

Target region for device code generation Device-host data management Conditional execution of code in device Target device selection during runtime

# **OpenMP 4.5 offloading**





**#pragma omp target map**(tofrom: myVar) **if**(myCondition) **device**(2) { myVar ++; }

### **Complex Test Cases**

#### ypedef struct node { double data; struct node \* next; node\_t; oid map\_ll(node\_t \*head) if (!head) return; pragma omp target enter data map(to:head[:1]) while(head->next) { // Note: explicit attachment node\_t \*cur = head->next; ragma omp target enter data map(to:cur[:1]) ragma omp target

head->next = cur id unmap ll(node t \*head) { if (!head) return; gma omp target exit data map(from:head[0].data) while (head -> next) { // Note: only copies back the data element to avoid overwriting next pointer

ma omp target exit data map(from:head[0].next[0].data)

define RealType double #define N 10

pragma omp declare target ass MyVector

> inline RealType operator()(int i, int j, int k) const return X[k+Length[2]\*(j+Length[1]\*i)];

inline RealType& operator()(int i, int j, int k) **return** X[k+Length [2]\*(j+Length [1]\*i)];

MyVector(int 1, int m, int n)

Length[0] = 1;Length[1] = m;Length[2] = nX = new RealType[l\*m\*n];

RealType \*& getData() { return X;

RealType \* getData() const { return X; int getSize() const { return Length[0]\*Length[1]\*Length[2]

int Length [3] RealType \* X

agma omp end declare targe

main () {

MyVector gamma (N, N, N) int size = gamma.getSize();

agma omp target enter data map(to:gamma) agma omp target enter data map(to:gamma.X[0:size]) map(to . Length )

ragma omp target for(int i = 0 ; i < N ; i++) for (int j = 0; j < N; j++) for (int k = 0; k < N; k++) gamma(i, j, k) = 1.0;

omp target exit data map(from:gamma.X[0:size]) for (int i = 0; i < N; i + +) for (int j = 0; j < N; j++) for (int k = 0; k < N; k++)

cout << gamma(i,j,k) << " return 0:

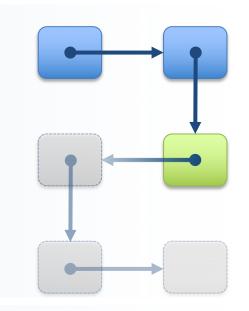


The *map\_ll* function (line 6) uses *target* enter data directive to first map the head of the linked list, followed by mapping the pointer to the next node of the list and assigning it on the device. The unmap\_ll (line 20) function explicitly copies the data using map(from:...) and target exit data.

#### **Deep Copy of Classes:**

This code came from analyzing a full scale ECP application. It uses the *declare target* directive (line 4 to 36) to ensures that procedures and global variables can be executed and data can be accessed on the device. When the C++ methods are encountered, device-specific versions of the routines are created that can be called from a target region.

Deep copy is performed through the use of target enter data (lines 43 and 44) by first mapping the class and then the individual class members. Computation is performed on the device (line 46). After computation is over, the data is copy back to the host (line 52).



nt test\_map\_device()

} // end target
} // end target data

/ checking results

errors = 0;

return errors;

static double VAR; B() {}

\* res = B::VAR;

double exp = 1.0, res = 0.0;

for (int i = 0; i < N; ++i) in\_1[i] = 1; }

for (int i = 0; i < N; ++i) in\_2[i] = 2; }

for (int i = 0; i < N; ++i)

shared (sum,  $h_array$ ) for (int i = 0; i < N; ++i)

sum += h\_array[i];

pragma omp taskwait

errors = 2.0 \* N != sum

pragma omp target enter data nowait

depend(in: in\_1) depend(in: in\_2)

h\_array[i] = in\_1[i] \* in\_2[i]; }

pragma omp target exit data nowait \

agma omp task depend(in: h\_array)

uble B::VAR = 1.0

t test\_static()

int errors = 0

B::modify(&res)

eturn errors;

ouble sum = 0.0;

errors = res != exp

class B {

int num\_dev = omp\_get\_num\_devices(), sum[num\_dev], error int \* h\_matrix = (int \*) malloc(num\_dev \*N\* sizeof(int));

omp target data map(from: h\_matrix[dev\*N:N]) device(dev)

omp target map(from: h\_matrix[dev\*N:N]) device(dev)

for (int dev = 0; dev < num\_dev; ++dev) {</pre>

for (int i = 0; i < N; ++i) h\_matrix [dev \*N + i] = dev;

for (int dev = 0; dev < num dev; ++ dev)  $sum[dev] = h_matrix[dev*N + 0];$ 

for (int i = 1; i < N; ++i) sum[dev] += h\_matrix[dev\*N + i]

errors |= (dev \* N != sum[dev]);

static void modify (double \* res) {

pragma omp target map(tofrom: res[0:1])

double + h\_array = (double +) malloc(N + sizeof(double))
double + in\_1 = (double +) malloc(N + sizeof(double));

double \* in\_2 = (double \*) malloc(N \* sizeof(double))

pragma omp task depend(out: in\_1) shared(in\_1)

pragma omp task depend(out: in\_2) shared(in\_2)

map(alloc: h\_array[0:N]) map(to: in\_1[0:N])
map(to: in\_2[0:N]) depend(out: h\_array) \

gma omp target nowait depend(inout: h\_array)

map(from: h\_array[0:N]) depend(inout: h\_array

My Vector Attributes Methods σ 0 P decl target tar dmo dmo

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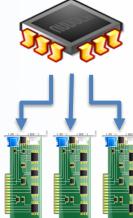
#pragma

#pragma

# Simple Test Cases

#### **Offloading Multiple devices:**

Each row of the matrix to each of the available devices. Use the *device* clause to select a device for data movement and computation. Target data region maps a portion of the matrix to each device (line 6). Target region does the computation (line 8)



#### Mapping static attribute of a class:

The unique value of the static VAR is default mapped inside the method of a class with a target region (lines 6-9). An OpenMP 4.5 capable compiler should capture the static variable (VAR) and map it to and from the device.

#### **Task dependencies:**

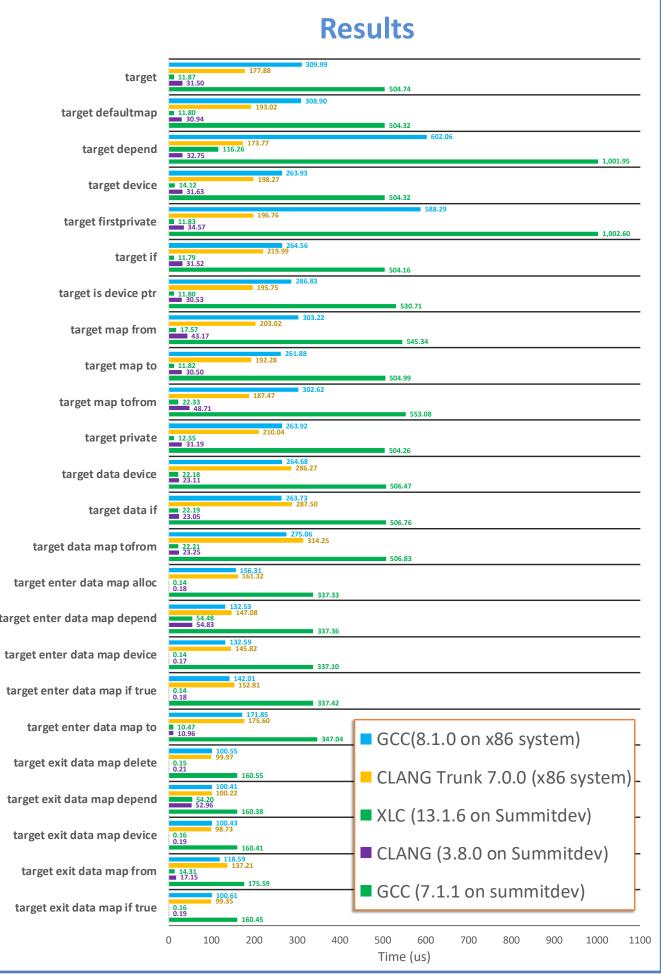
Task graph composed of host tasks and target tasks that have in and out dependencies between each other. Asynchronous behavior is specified using the nowait clause. Data map tasks are separated from computation tasks.

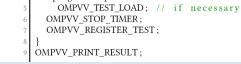
# Line 1 Sum **O** Host O Device

# Specification coverage evaluation

We are currently developing a test suite to asses the level of coverage of the OpenMP 4.5 specifications by the different compiler implementations. We have put together a methodology that guarantees full coverage of the specification as well as correct test implementation. We currently have released over 64 tests and we are currently in the process of releasing 33 more tests that are under review.







OMPVV\_START\_TIMER;

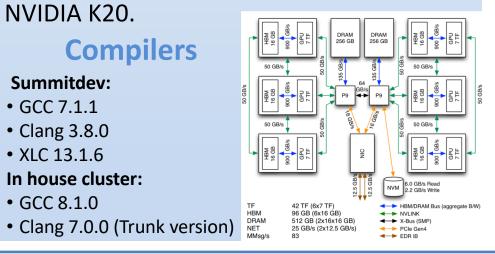
OMPVV INIT TEST;

#pragma omp

Measuring runtime overhead with multiple executions of different openMP directives and clauses. Each experiment consist of 1002 runs, removing the max and min and taking the average value.

#### **Testing systems**

Two different systems and 5 different compilers and versions were tested. Summitdev features IBM S822LC nodes with POWER8 processors. Each node has a total of 160 hardware threads, 256 Gb of DRAM and as target devices, 4 NVIDIA Tesla P100 GPUs. The second system is an in-house cluster where each node features two Intel(R) Xeon(R) CPU E5-2670 with 32 Hardware threads, 64 Gb of DRAM and one



#### **Systems**

System	Model	Processors	Cores/node	Threads/node	Memory	Accelerator	Complers
Titan	Cray XK7	AMD Opteron 6274	16	16	32 GB	1 NVIDIA K20X	CCE 8.7.2
Summitdev	IBM S822LC	2x Power8	20	160	256 GB	4 NVIDIA P100	GCC 7.1.1 Clang 3.8.0 XLC 13.1.6
Summit	IBM AC922	2x Power9	42	168	512 GB	6 NVIDIA V100	Clang 3.8.0 XLC 13.1.7

#### **Results summary**

	Summitdev					Summit		Titan
	GCC	gfortran	Clang	XLC	XLF	Clang	XLC	CCE
OpenMP 4.5 Feature	7.1.1	7.1.1	3.8.0	13.1.6	15.1.7	3.8.0	13.1.7	8.7.2
target	14/14	13/13	14/14	13/14	12/13	12/14	11/14	13/14
target data	5/6	4/4	6/6	6/6	2/4	6/6	6/6	3/6
target enter/exit data	6/7	-	6/7	6/7	-	6/7	6/7	5/7
target enter data	6/7	-	6/7	6/7	-	6/7	6/7	5/7
target update	5/5	-	5/5	4/5	-	5/5	4/5	4/5
target teams distribute	10/11	-	8/11	10/11	-	-	-	9/11
target teams distribute parallel for	13/14	-	11/14	11/14	-	-	-	10/14





